REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 30-38 are presently active in this case, Claims 30-38 having been added by way of the present Amendment. No new matter has been entered. (See, e.g. page 12, lines 12-16, page 15, lines 18-22, and the figures.) Claims 1-29 have been canceled without prejudice or disclaimer.

In the outstanding Official Action, Claims 1-3 were rejected under 35 U.S.C. 103(a) as being unpatentable over Ueno et al. (U.S. Pub. No. 2003/0008075) in view of Yamato et al. (U.S. Patent No. 6,388,201). Claims 4 and 5 were rejected under 35 U.S.C. 103(a) as being unpatentable over Kato (U.S. Pub. No. 2002/0030978) in view of Ueno et al. Claims 16-29 were rejected under 35 U.S.C. 103(a) as being unpatentable over Ueno et al. in view of Yamato et al. and further in view of Kato.

The Applicant notes that Claims 1-5 and 16-29 have been canceled without prejudice or disclaimer, thereby rendering the above rejections moot. The Applicant further submits that new Claims 30-38 are allowable over the cited art forth reasons set forth below.

The basic requirements for establishing a *prima facie* case of obviousness as set forth in MPEP 2143 include (1) there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings, (2) there must be a reasonable expectation of success, and (3) the reference (or references when combined) must teach or

suggest all of the claim limitations. The Applicant submits that a *prima facie* case of obviousness cannot be established in the present case because the references, either when taken singularly or in combination, do not teach or suggest all of the claim limitations, and there is no suggestion or motivation to modify or combine the references in the manner suggested to arrive at the present invention.

Independent Claims 30, 35, and 37 each recite a thin-film transistor comprising a source region and a drain region which are provided with an interval on an insulating substrate, a gate insulator layer which is provided over the interval between the source region and the drain region, *a gate electrode which is provided on the gate insulator layer*, and a source electrode and a drain electrode which are provided on the source region and the drain region, respectively. Claim 30 recites that the gate electrode comprises a first metal diffusion-preventing layer formed on the gate insulator layer, a metal seed layer formed on the first metal diffusion-preventing layer, a metal layer formed on the metal seed layer, and *a second metal diffusion-preventing layer covering the exposed surface including the side surface of the multilayered structure having the metal seed layer and the metal layer, and wherein the metal seed layer and the metal layer are surrounded by the first metal diffusion-preventing layer and the second metal diffusion-preventing layer, and have a forward tapered cross section.* Claim 35 recites that the gate electrode comprises a first metal diffusion-preventing layer formed on the gate insulator layer, a metal seed layer formed on the first metal diffusion-preventing layer, a metal layer formed on the metal seed layer and *having a forward tapered cross section*, and *a second metal diffusion-preventing layer*

covering the exposed surface including the side surface of the multilayered structure having the metal seed layer, the metal layer and the first metal diffusion-preventing layer, and wherein the metal seed layer and the metal layer are surrounded by the first metal diffusion-preventing layer and the second metal diffusion-preventing layer. Claim 37 recites that the gate electrode comprises a first metal diffusion-preventing layer formed on the gate insulator layer, a metal layer formed on the first metal diffusion-preventing layer, and *a second metal diffusion-preventing layer covering the exposed surface including the side surface of the multilayered structure having the metal layer and the first metal diffusion-preventing layer, and wherein the metal layer is surrounded by the first metal diffusion-preventing layer and the second metal diffusion-preventing layer, and has a forward tapered cross section.*

The Ueno et al. reference relates to a dual damascene process, and the structure of the invention of the Ueno et al. reference is that of a metal wiring layer (11) that is formed directly on a diffusion prevention layer (15). The diffusion prevention layer (15) is formed of nickel, etc., which is applied to SiO_2 subjected to a catalytic treatment, using an electroless plating method. Further, the Ueno et al. reference describes that a feature of the invention is that the wiring layer (11) is formed directly on the diffusion prevention layer (15) by using the electroless plating (or electrolytic copper plating) method. Therefore, the Ueno et al. reference proposes that a seed layer (conductive layer), which was necessary to form a copper wiring layer in the conventional manufacturing method, becomes unnecessary.

In the Official Action, FIG. 1 of Ueno et al. reference is cited for showing a seed layer as the prior art. With regard to the depiction in FIG. 1, the Ueno et al. reference indicates that

although a dual damascene process is used, the diffusion prevention layer and the seed layer are formed by a dry process that uses a sputtering apparatus. Therefore, there arises a problem in simplifying the process and reducing the cost. The Ueno et al. reference also describes that it is hard to form the diffusion prevention layer by an electroless plating process.

As compared to the present claims, the Ueno et al. reference fails to disclose the following features:

(a) providing a second metal diffusion-preventing layer covering the exposed surface including the side surface of the multilayered structure having at least the metal layer;

(b) the metal layer has a forward tapered cross section (see page 15, lines 18-22, of the present application);

(c) the structure of (a) is applied to the gate electrode, which is provided on the gate insulating layer between the source electrode and the drain electrode in the thin-film transistor (TFT); and

(d) the structure of (a) is applied to the wiring of the gate electrode, which electrically connects elements of the gate electrode, the source electrode, and the drain electrode.

Regarding feature (a), in the wiring structure of the Ueno et al. reference, the surface of the wiring is provided with a cap insulator layer (SiN, SiO_2). The wiring of the Ueno et al. reference does not have the metal diffusion-preventing function of the present invention. The structure of the present invention is to cover the metal layer (and metal seed layer) with a metal diffusion-preventing layer, and to improve the resistance pressure which prevents the

diffusion of the metal from the metal layer (and metal seed layer).

Regarding feature (b), the wiring layer of the Ueno et al. reference has an inverted L-shaped cross section, and not a forward tapered cross section, as claimed in the present application. The metal layer of forward tapered cross section of the present invention reduces a short in the wiring provided on the upper metal layer, and improves coverage of the interlayer insulator, which is deposited after the metal layer is formed.

Regarding features (c) and (d), although the Ueno et al. reference describes a wiring layer, it does not disclose using the wiring layer in an electrode of a transistor element as in the present invention. Further, the manufacturing method of the Ueno et al. reference does not comprise manufacturing steps which take into consideration the formation of electrodes. The present application describes the use of a photoresist layer in order to form the electrodes having the form as claimed.

The Applicant further submits that the Yamato et al. reference and the Kato reference fail to supplement all of the above noted deficiencies in the teachings of the Ueno et al. reference.

The Official Action indicates that Yamato et al. depicts in FIG. 6(e) a second metal diffusion-preventing layer that covers the exposed surface including the side surface of a multilayered structure. However, FIG. 6(e) shows that the three surfaces of the conductive layer (14) of square-shaped cross section are covered by metal coating (22). The other surface is covered by a ground (20), and a base layer (13) formed of an insulator is provided at the bottom surface of the ground (20). Further, the Yamato et al. reference depicts a

magnetic head part that is provided with a cover layer (18) formed of polyimide resin on the metal coating (22). Note also exposed terminal forming portion (36), plated with metal plated layers (19).

There is no description in the Yamato et al. reference of providing a "second metal diffusion-preventing layer" as asserted in the Official Action. Rather the Yamato et al. reference describes a wiring structure which is intended to prevent a short circuit in the metal terminal layer and the metal supporting layer. Thus, the Yamato et al. reference does not disclose feature (a) noted above, as is recited in the claims of the present application.

Furthermore, the cross section of the conductive layer (14) shown in FIG. 6(e) of the Yamato et al. reference is square-shaped, and Yamato et al. reference does not provide a description of a wiring layer having a forward tapered cross section. Thus, the Yamato et al. reference does not disclose feature (b) noted above, as is recited in the claims of the present application.

In addition, the Yamato et al. reference does not disclose providing a metal diffusion-preventing layer on the gate insulating layer between the source electrode and the drain electrode in the thin-film transistor (TFT) as in the present invention.

Accordingly, even if the Ueno et al. reference is combined with the Yamato et al. reference, the combined invention is different from the presently claimed invention. Thus, a *prima facie* case of obviousness cannot be established with respect to the claims of the present application based upon the combination of the Ueno at al. reference and the Yamato et al. reference.

Furthermore, the Applicant submits that the Kato reference does not supplement the deficiencies in the teachings of the Ueno et al. and Yamato et al. references noted above.

The Kato reference proposes reducing the weight of a substrate by forming a radial wiring on the substrate and reducing the amount (area) of the conductor pattern covering the entire mounting region.

The Kato reference does not describe electrodes of driving elements that are surrounded by the first and second metal diffusion-preventing layers, which are distinctive features of the present invention. Additionally, the Kato reference does not disclose applying a metal diffusion-preventing layer on the gate insulating layer between the source electrode and the drain electrode in the thin-film transistor (TFT) as in the present invention. Accordingly, there is no disclosure or concept of such application as in the present invention.

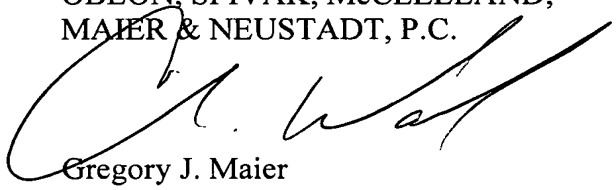
Accordingly, even if the Ueno et al. reference is combined with the Yamato et al. reference and the Kato reference, the combined invention is different from the presently claimed invention. Thus, a *prima facie* case of obviousness cannot be established with respect to the claims of the present application based upon the combination of the Ueno at al. reference, the Yamato et al. reference, and the Kato reference.

Thus, for at least these reasons, the Applicant respectfully submits that independent Claims 30, 35, and 37 are allowable over the cited art. Furthermore, the dependent claims are considered allowable for the reasons advanced for the independent claim from which they respectively depend.

Consequently, in view of the above discussion, it is respectfully submitted that the present application is in condition for formal allowance and an early and favorable reconsideration of this application is therefore requested.

Respectfully Submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Gregory J. Maier
Registration No. 25,599
Attorney of Record

Christopher D. Ward
Registration No. 41,367

Customer Number

22850

Tel. (703) 413-3000
Fax. (703) 413-2220
(OSMMN 10/01)

GJM:CDW:brf
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